ABSTRACT

The invention relates to a TDM backplane bus system, in which a Frame Synchronisation signal is developed from an external communication signal, a data clock signal is produced from a free running clock oscillator independent of the FS signal, to select the frequency of said clock signal so that the number of periods within a frame is always at least one more than the number of timeslots required, to synchronise the FS signal to the CLK signal, and supply this synchronised Frame Synchronising signal (FS-S) to the TDM-bus. Further, said exceeding period(s) is identified by introducing a carry bit in the timeslot counters, said carry bit being set each time the counter(s) exceeds the number of timeslots on the TDM bus.